A novel architecture for DAQ in multi-channel, large volume, liquid Argon TPC.

B. Baibussinov, S. Centro, G. Meng, F. Pietropaolo,

S. Ventura

Università di Padova e INFN Sezione di Padova

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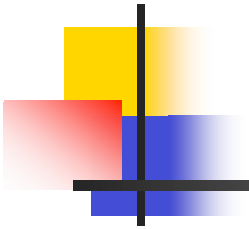
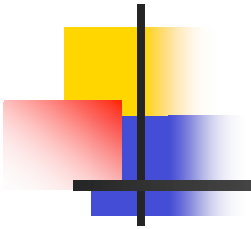


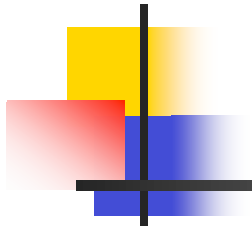
Outline

- Recently large interest has been shown for multi-ton LAr time-projection-chambers (TPC).
- In this paper we propose an architecture for DAQ based on components aimed to **high-resolution delta-sigma** conversion.
- This type of ADC is not at all popular in HEP experiments where the “events” are defined in time.
- In the TPC we have to deal with waveforms, limited in bandwidh, to be converted and recorded continuously, that is the typical case of delta-sigma ADC application.
- A **general scheme**, **simulations** on real signals, and results from a **prototype** will be shown.



Outline

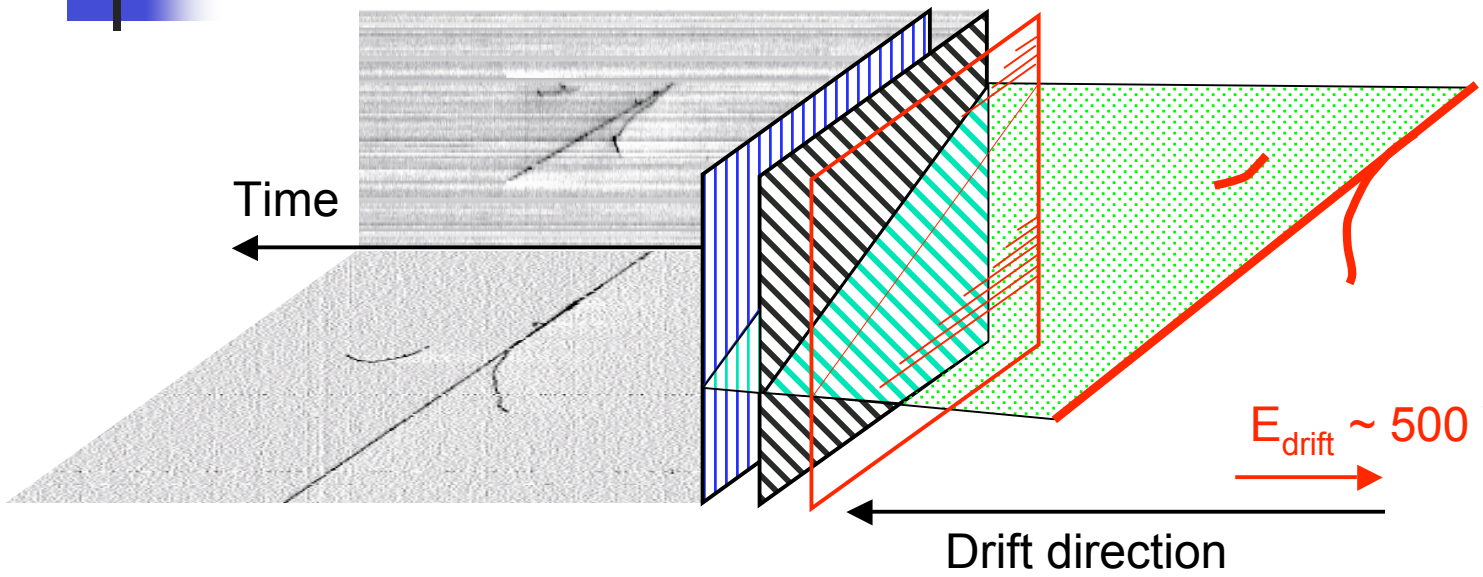
- The ICARUS front-end electronics
  - Layout in T600 module (analogue + digital)
  - Performance and limitations
- Alternatives solutions
  - Delta-Sigma modulator
  - Numerical filtering
- Summary

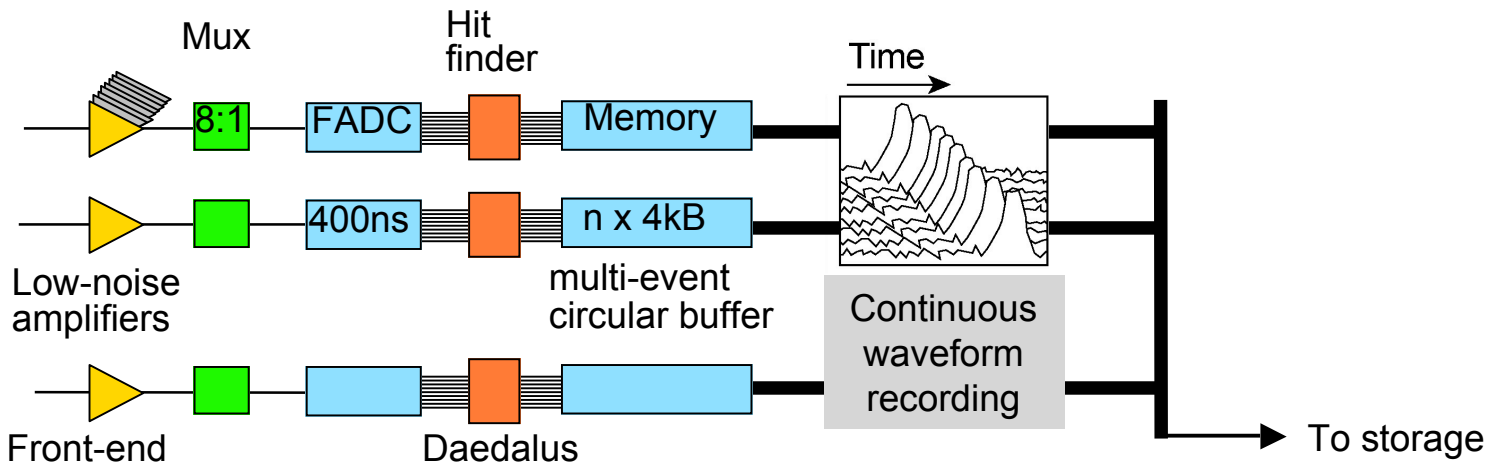


The ICARUS T600 experience

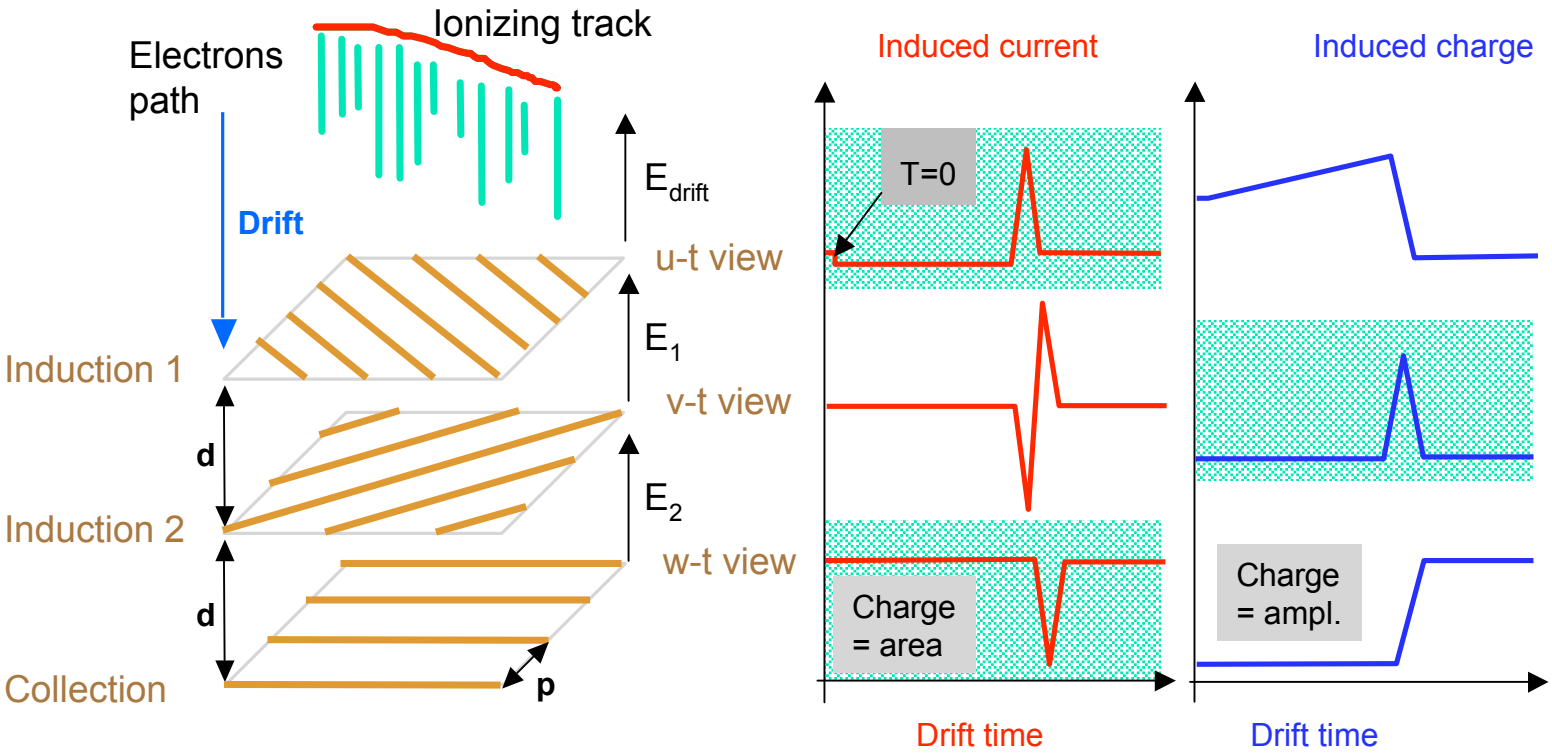
- The T600 DAQ system ($5 \cdot 10^4$ channels), designed in Padova, engineered and built by CAEN, has proven to perform satisfactory during the 2001 test run in Pavia.
- It consists of an analogue front-end followed by a multiplexed AD converter (10 bit) and by a digital VME module performing local storage, hit finding and data compression.
- From the experience gained with the T600 operation, an R&D phase is underway in view of an upgrade for a multi-kton detector with ~ $n \cdot 10^5$ channels (better S/N, larger integration, lower cost).

The ICARUS read-out principle





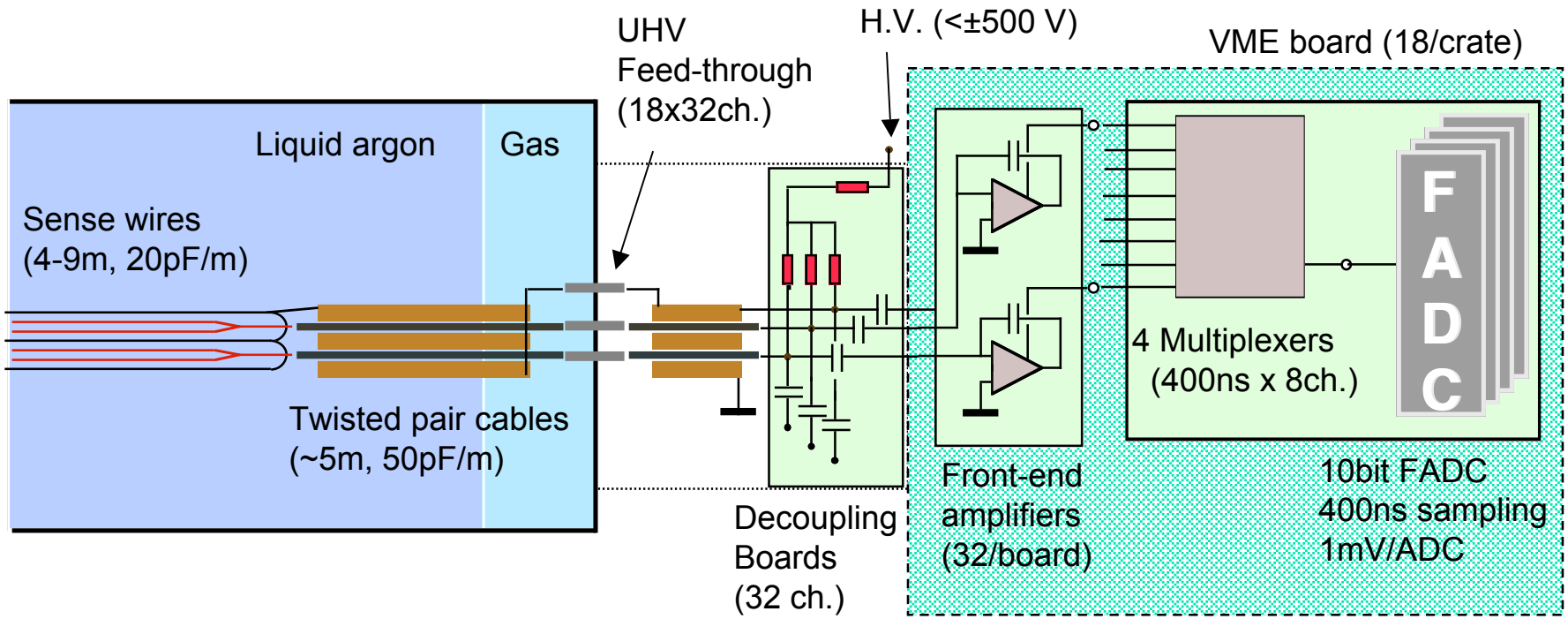
The induction signals



- ICARUS T600: three wire planes (pitch 3mm, separation 3mm)

E_{drift} = 500 V/cm
Mip signal ~ 12000 e^- (inc. recombinantion)
Electron drift velocity ~ 1.5 mm/μs
Typical grid transit time ~ 2-3 μs

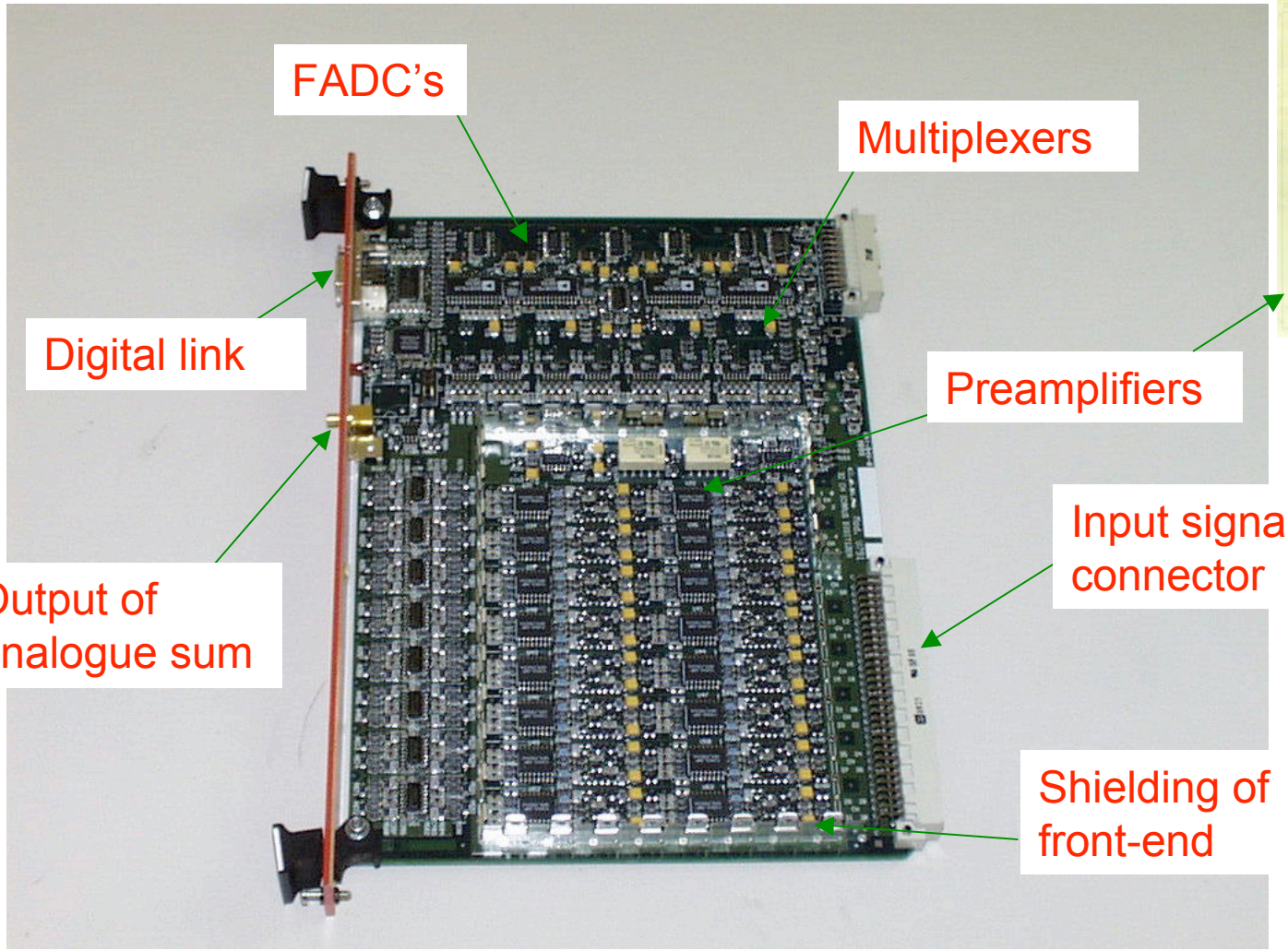
Layout of front-end electronics

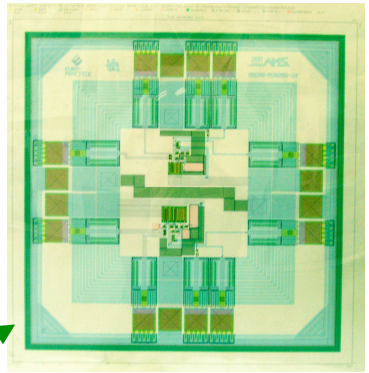


ICARUS T600: ~ 54000 channels — 1720 boards — 96 crates
Cost of the full electronic chain: ~ 80 € / channel

The T600 electronic racks

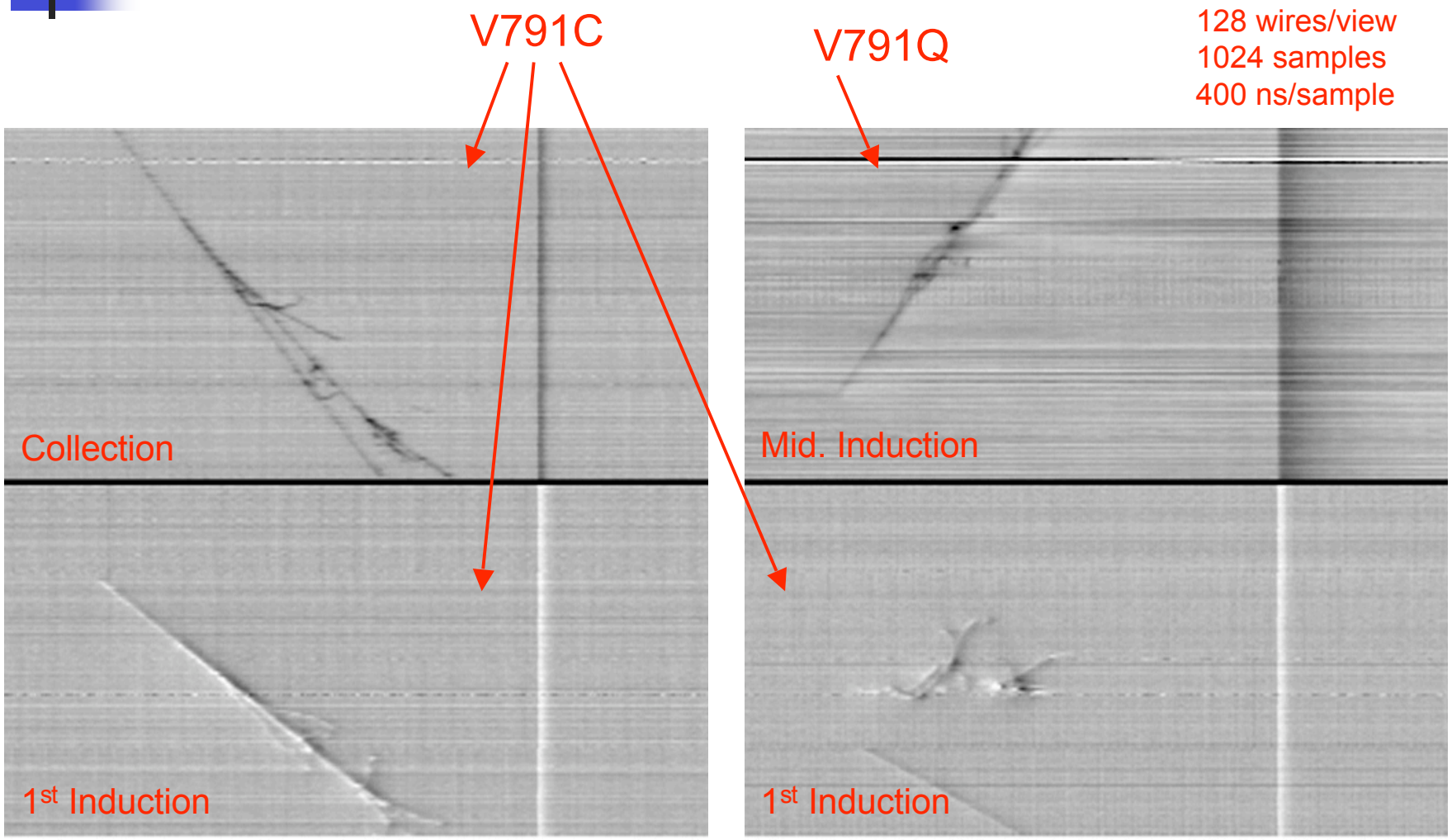
The analogue board V791





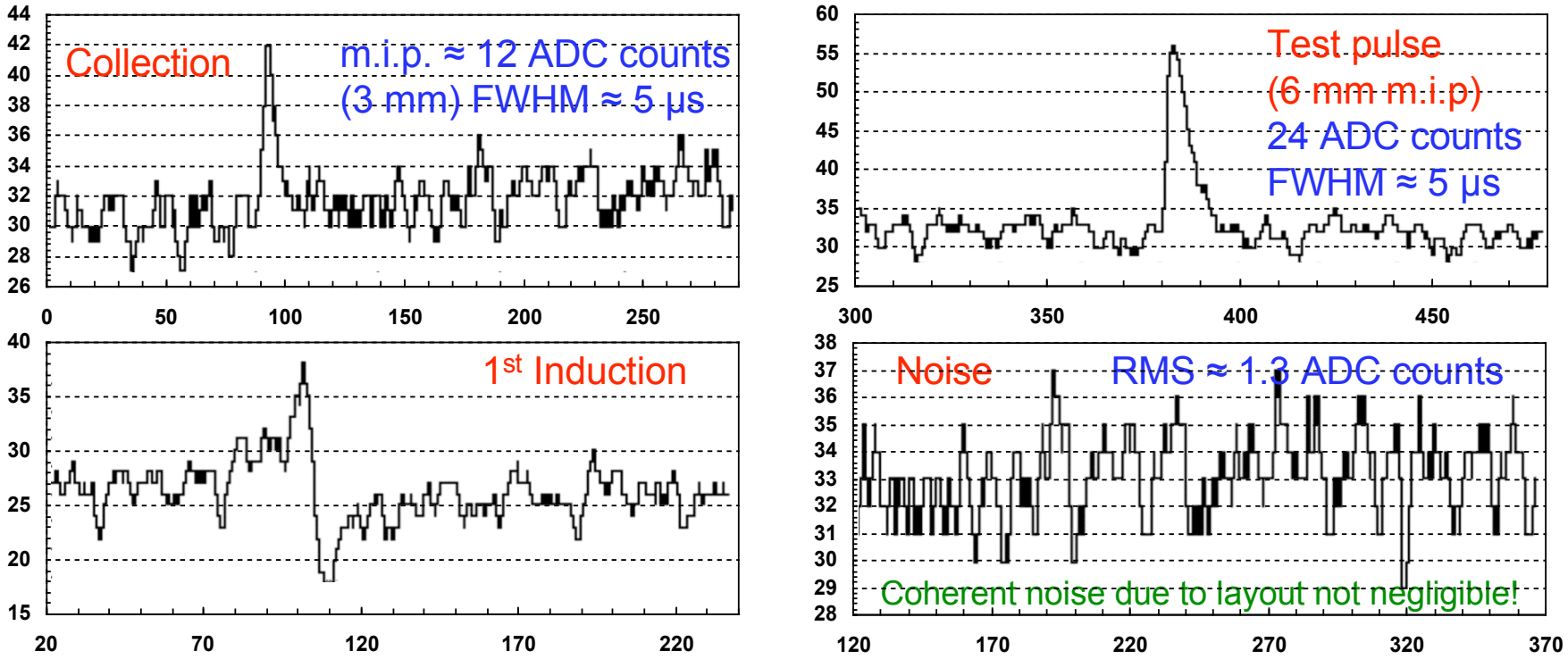
BiCMOS IC layout

Performance of the V791 boards



Performance of the V791C board

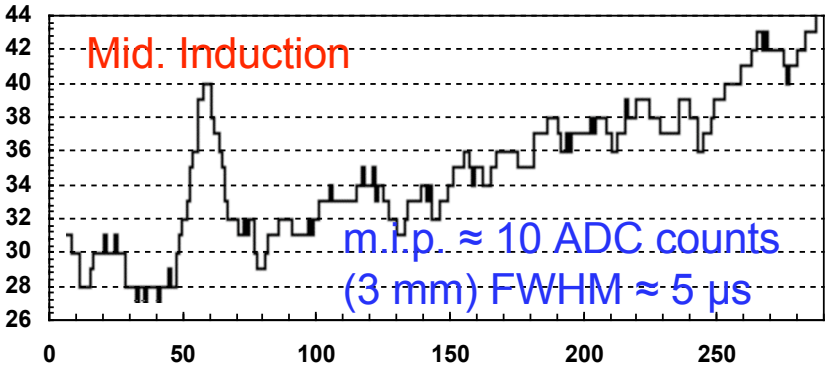
- Single wire waveforms (horiz. axis unit = 400 ns)

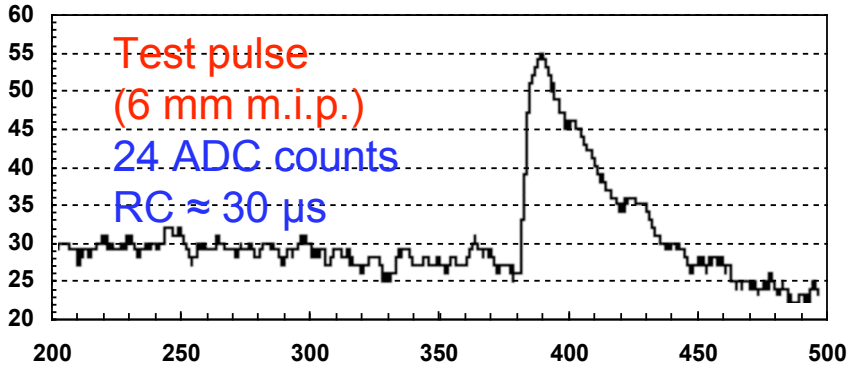


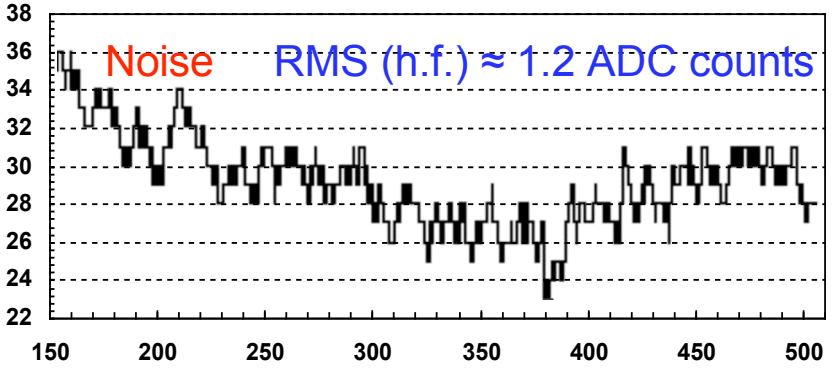
- RMS noise on T600 = 1.3 - 1.7 ADC counts (due to difficult environment in Pavia)

Performance of the V791Q board

- Single wire waveforms (horiz. axis unit = 400 ns)



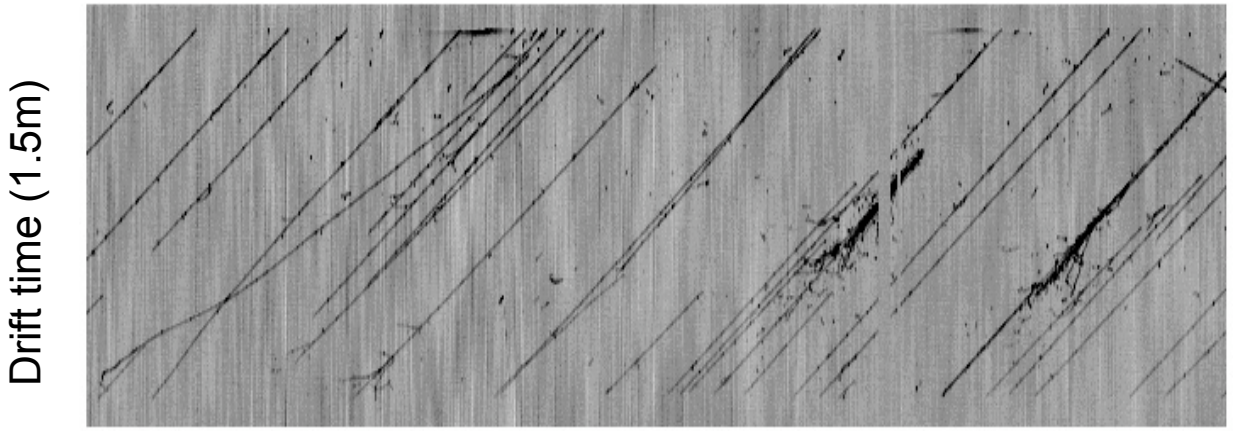




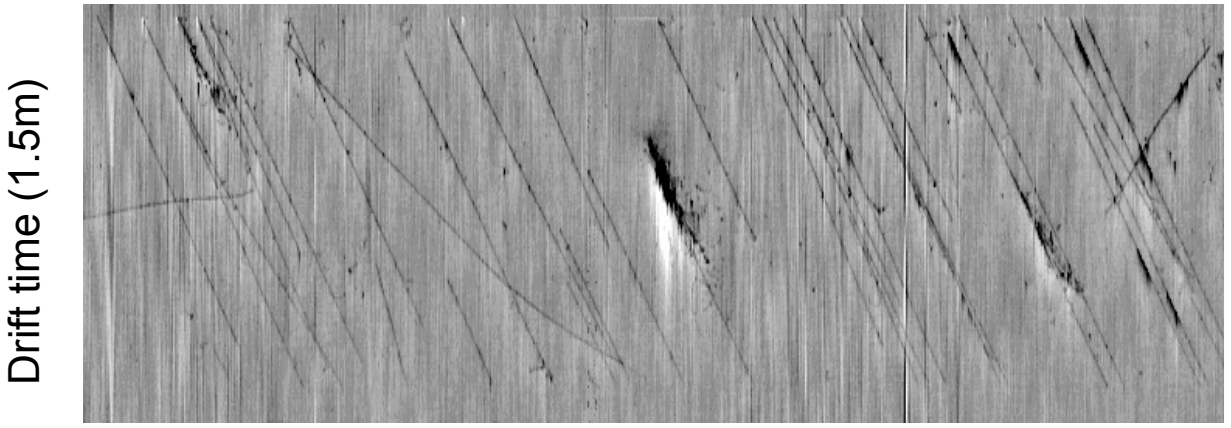
- Pulse height & shape from mid. plane wires very similar to those from collection plane wires.
- High frequency S/N also comparable.
- Low frequency minimized by baseline restorer.

Low frequency noise visible but not dangerous!

Events from T300 semi module



Collection view

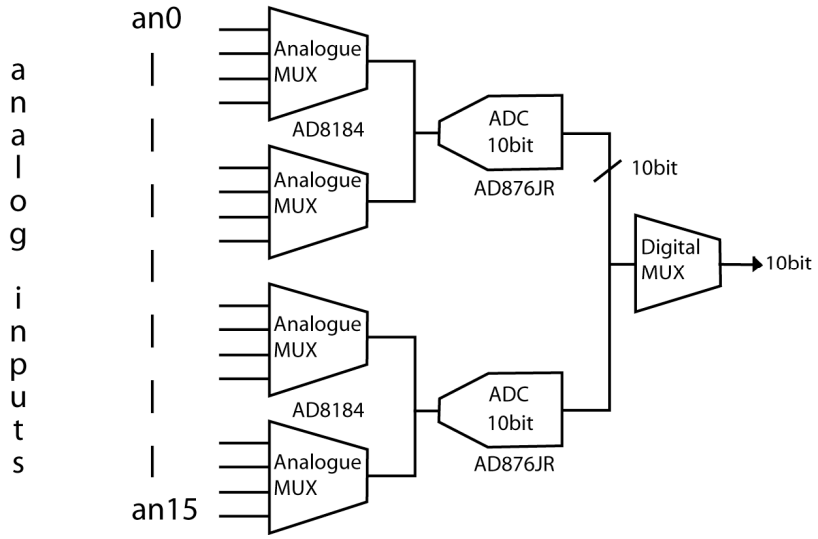


Induction2 view

Analog-to-digital conversion

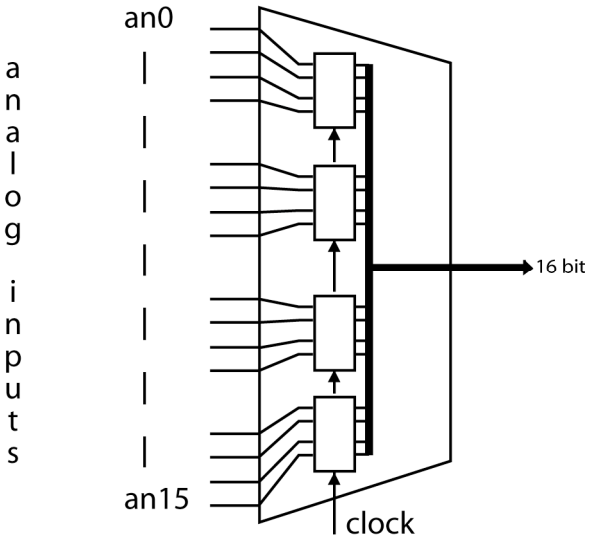
- Present architecture
  - Serves sets of 16 channels through analogue multiplexers and 10 bit FADC's
  - Trade-off between sampling speed and price
- FADC sampling rate 20MHz interleaved
  - 400 ns sampling time / channel
  - 40MHz digital output
- Dissipated power ~ 500 mW
- Not negligible components **count & cost**

- Two sets per V789 board (32 ch.)
  - Total bandwidth = 800 Mbit/s



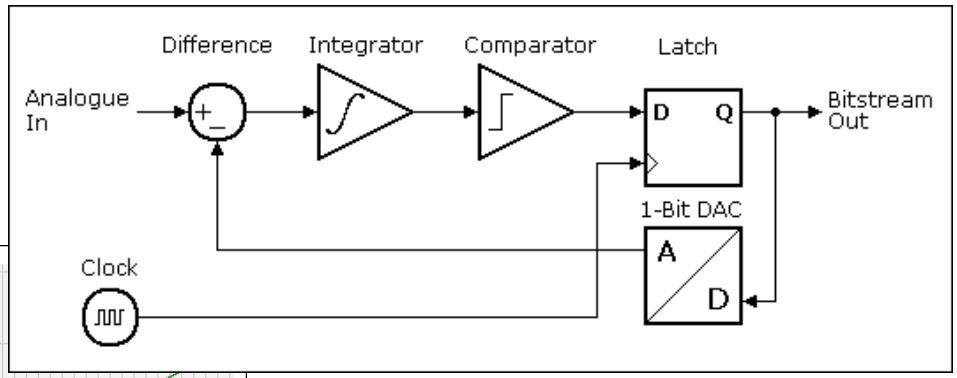
Compact serial AD converter

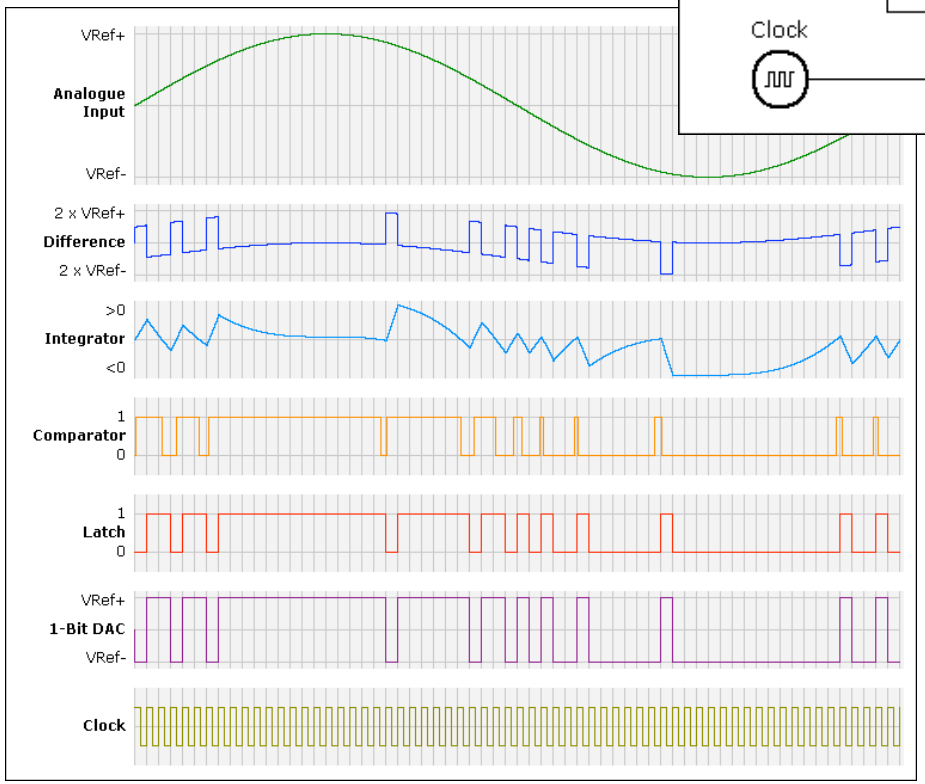
- New architecture based on 1-bit Delta-Sigma modulator
  - Interesting characteristics
    - No need for multiplexing
    - Very low number of components
    - Resolution better than 10 bit
    - Commercially available chip
    - Low price (< 1 € / channel)
  - Basic structure
    - Four QUAD FLATPACK 4x4 mm^2 components plus few glue logic
    - Sampling rate = 16 MHz
    - Dissipated power = 400mW
- Data reconstruction
  - Simple FIR filters could be implemented
    - In pipeline on FPGA / DSP
    - Off line after data storage
  - Serving multiples of 16 channels



First order Delta-Sigma modulator

http://www.beis.de/Elektronik/





1st order Delta-Sigma modulator

The latch is clocked at the modulation clock frequency, and for a given constant input signal, a periodic sequence of 0 and 1 is obtained. The duty cycle of the output digital value will change if the input signal changes.

The main feature of this technique is to move into digital domain all the conversion process at a very early stage and to exploit the use of numerical digital filtering techniques.
The final quality of the converted data is highly dependent on the sampling frequency and numerical filtering.

2nd order Delta-Sigma modulator

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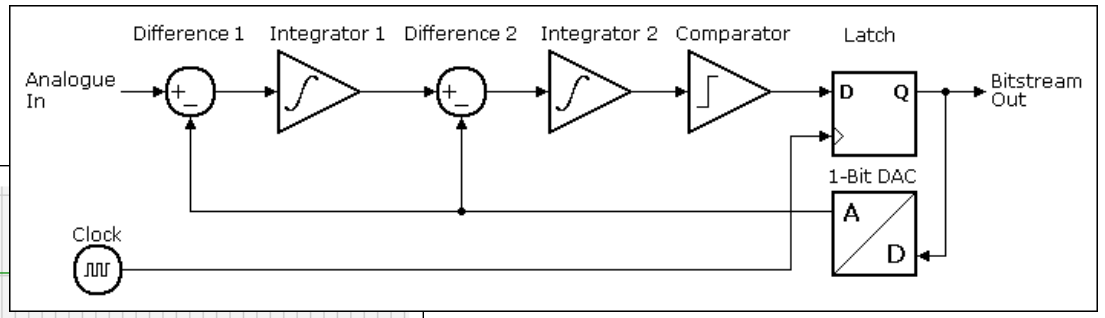
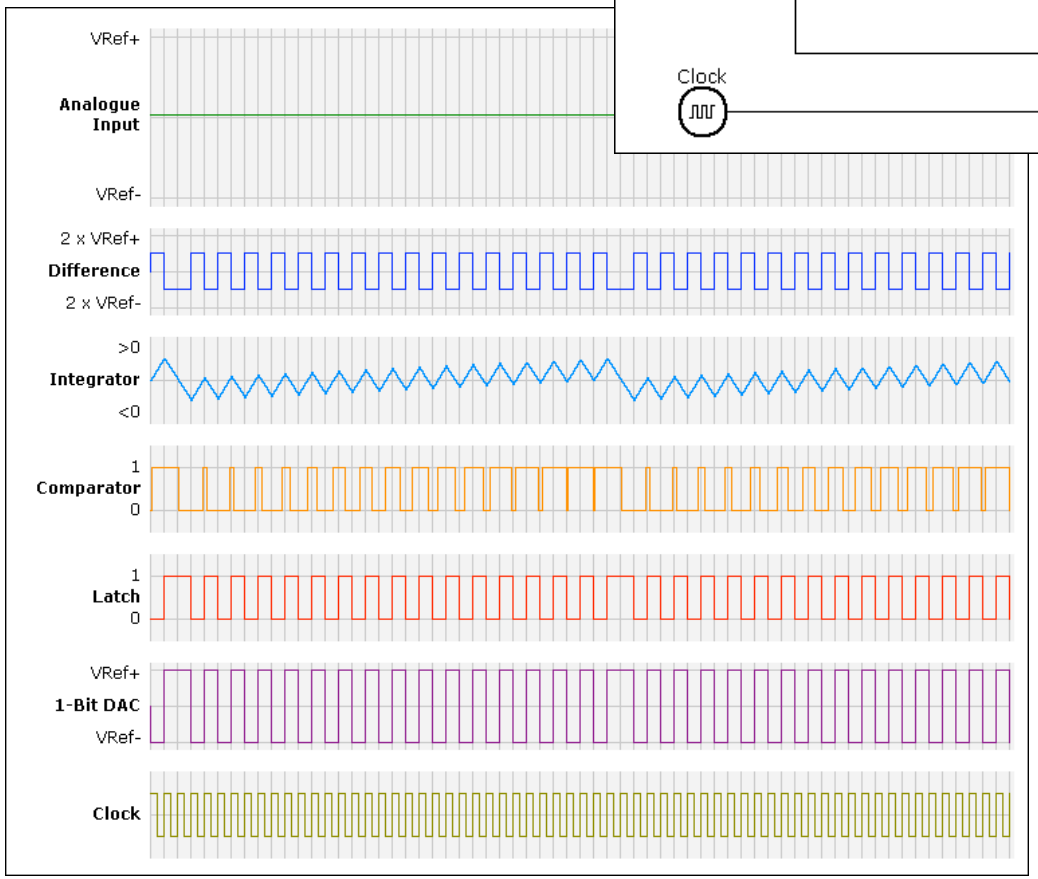
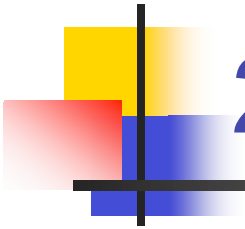






2nd order Delta-Sigma modulator

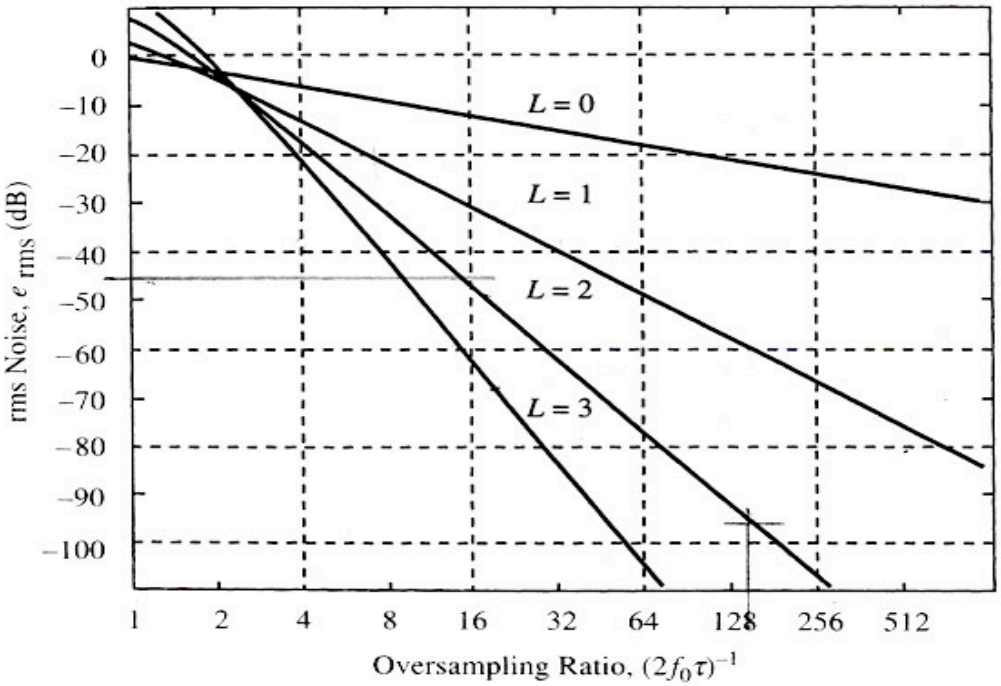
The bit-stream of such a modulator is much closer to the ideal pulse proportion signal than 1st order so that:

_ either the input signal bandwidth may be higher,
_ or the clock rate may be lower,
_ or the output precision is increased (less noise).

Additionally "non-random noise" is avoided to a great extent.

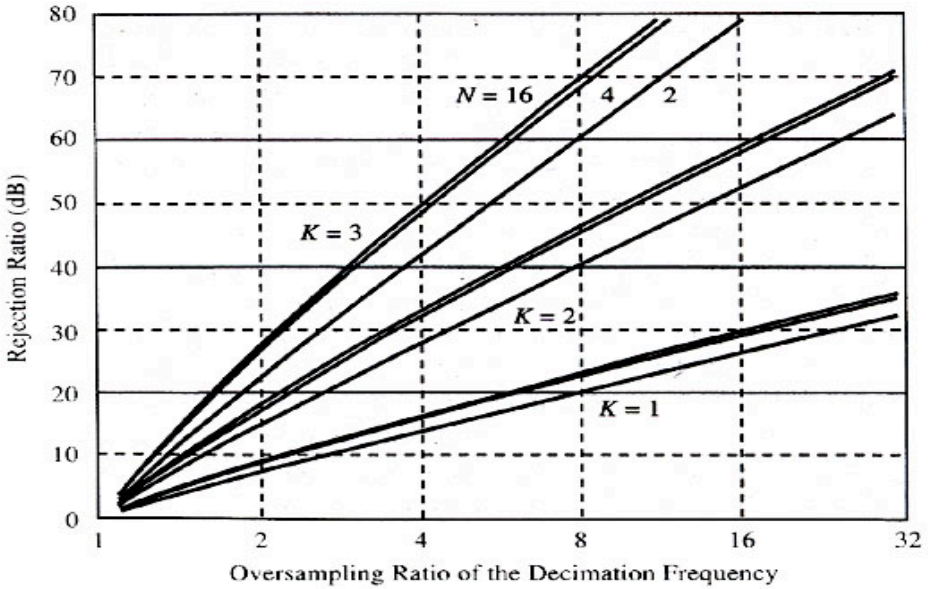
The residual **tones**, present in 1st order are almost negligible.

2nd order Delta-Sigma modulator



The rms noise that enters the signal band for oversampling ratios in the range 1 through 512, assuming busy input signals. Graphs are plotted for ordinary quantization without feedback $L = 0$, and first-, second-, and third-order $\Delta\Sigma$ quantization. 0 dB of noise corresponds to that of PCM sampled at the Nyquist rate. A common level spacing is used in all the quantizers.

2nd order Delta-Sigma modulator



A graph of

$$\frac{\text{sinc}^k\{\pi(f_D - f_0)NT\}}{\text{sinc}^k\{\pi(f_D - f_0)T\}}$$

It is attenuation of out-of-band components of the signal at frequency $f_D - f_0$ for sinc^k decimation; N is the decimation ratio $N = f_s/f_D$. This attenuation should meet the antialiasing requirement of the application. In Section 1.4.2 we show how this graph can be used to measure the attenuation of an interpolator.

Reconstruction Filter & decimator

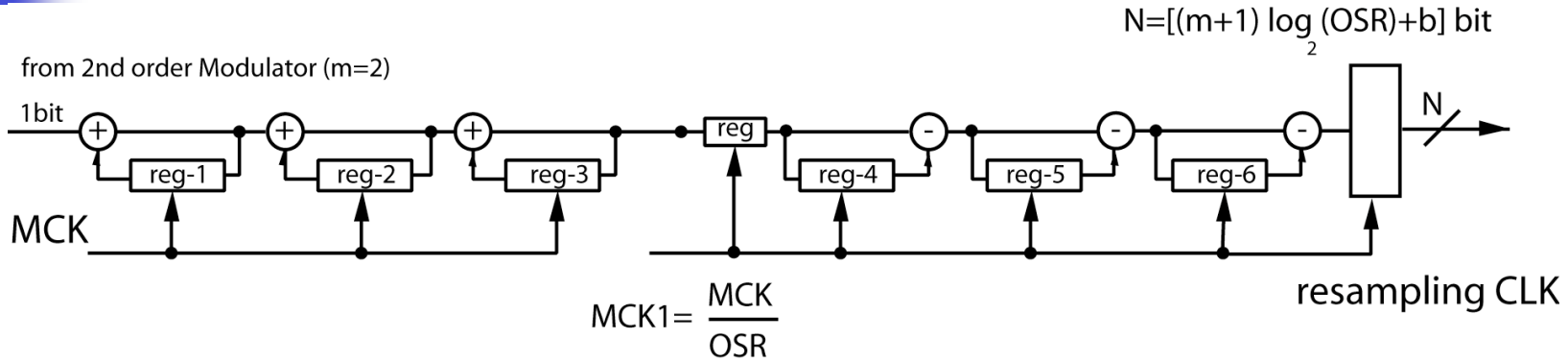
Windowed **sinc** [sin(x)/x] filters are used to reconstruct the signal inside a given bandwidth. They are very stable, and easy to implement both software or hardware.

General form for **sinc***K*

$$H(z) = \left(\frac{1}{M} \frac{1 - z^{-M}}{1 - z^{-1}} \right)^{K}$$

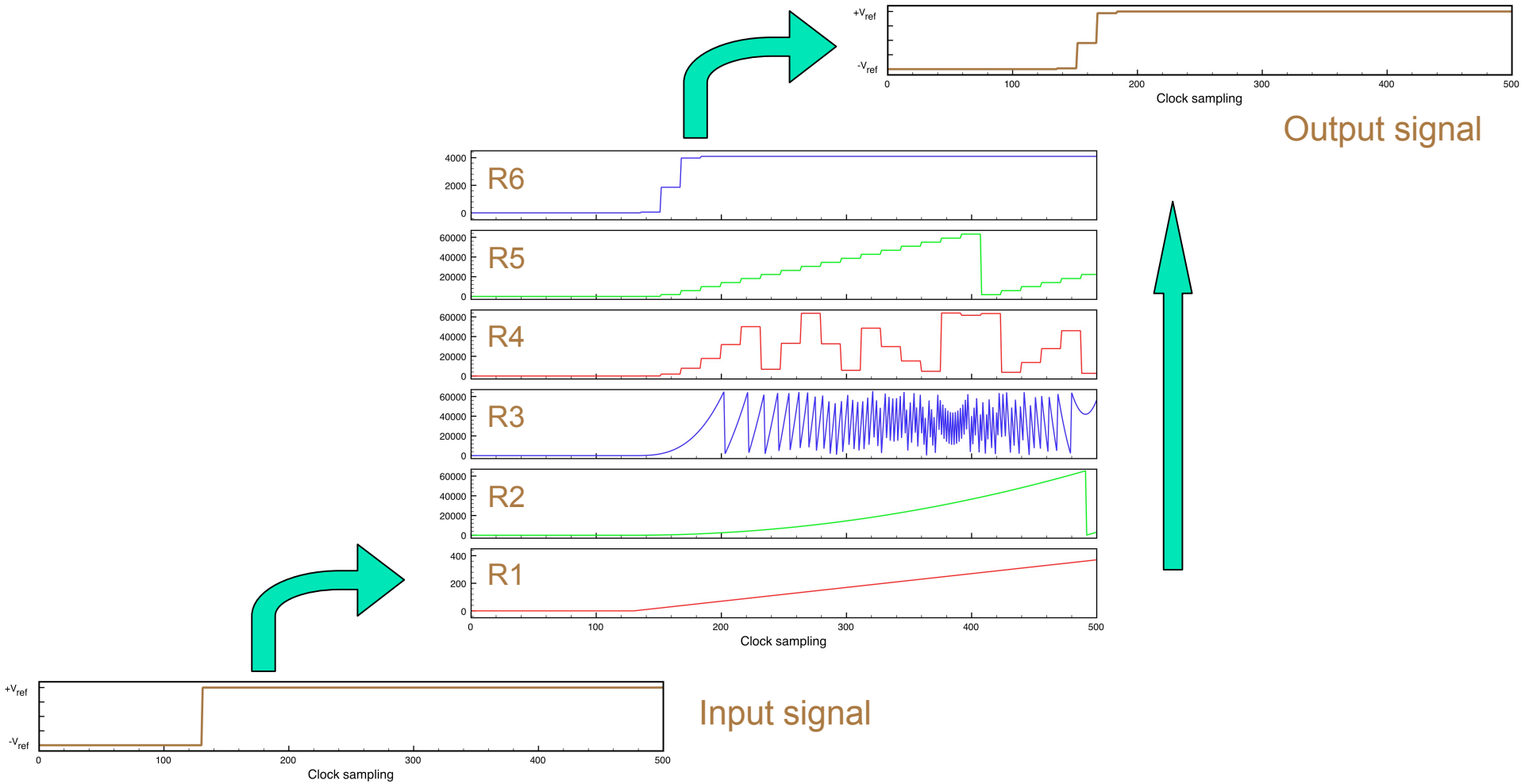
Where *M* is the window width. We adopted *k*=3

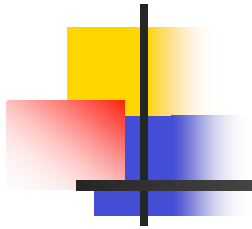
Reconstruction Filter & decimator



In the given scheme there is the discrete implementation of the **sinc*3*** FIR (Finite Impulse Response) comb filter that operates on a sliding window of bits which length is defined by the OSR factor (oversamplig ratio).
The width of the data (N) is obviously related to the OSR.

Data reconstruction (OSR=16)



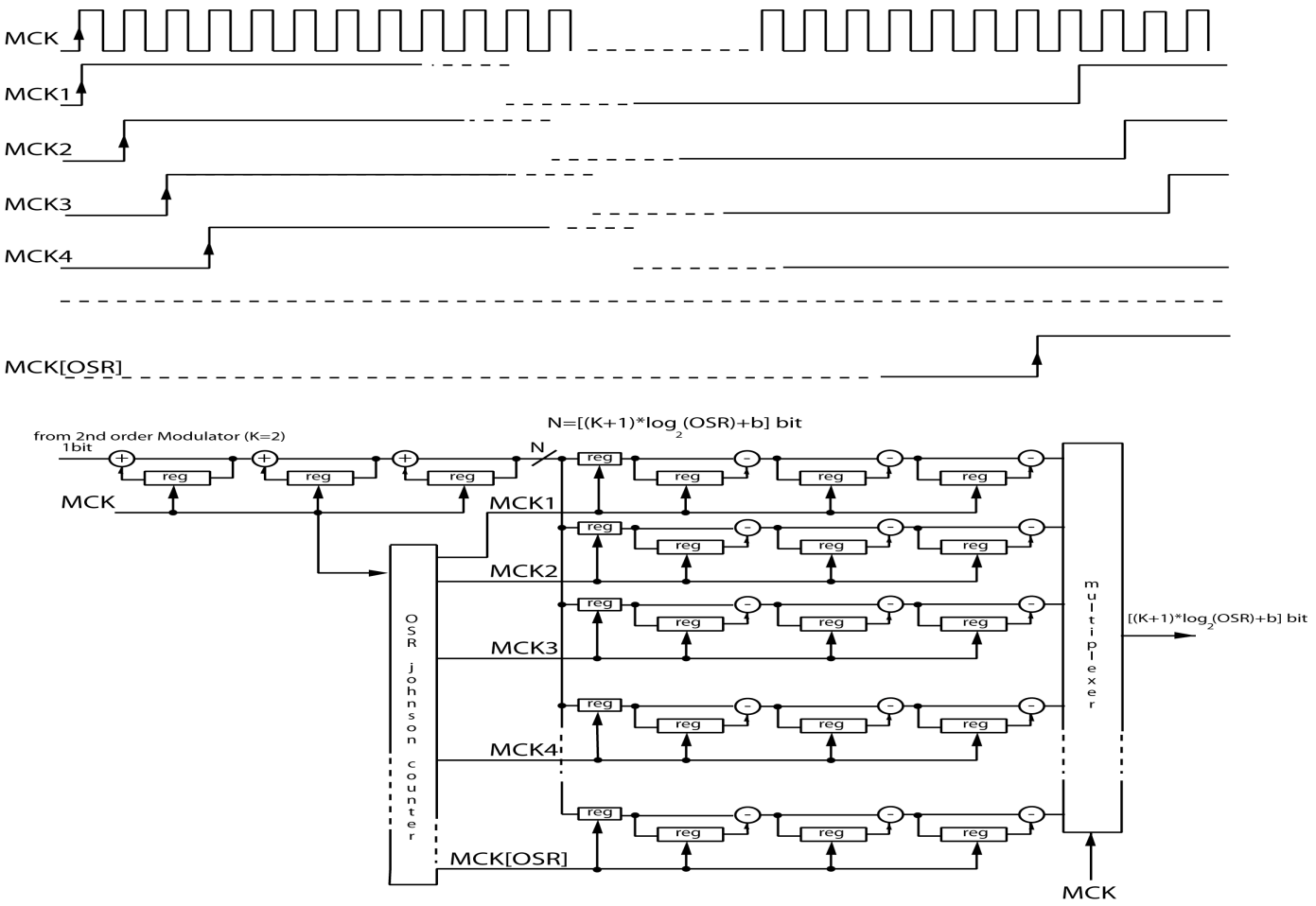


Filter & decimator

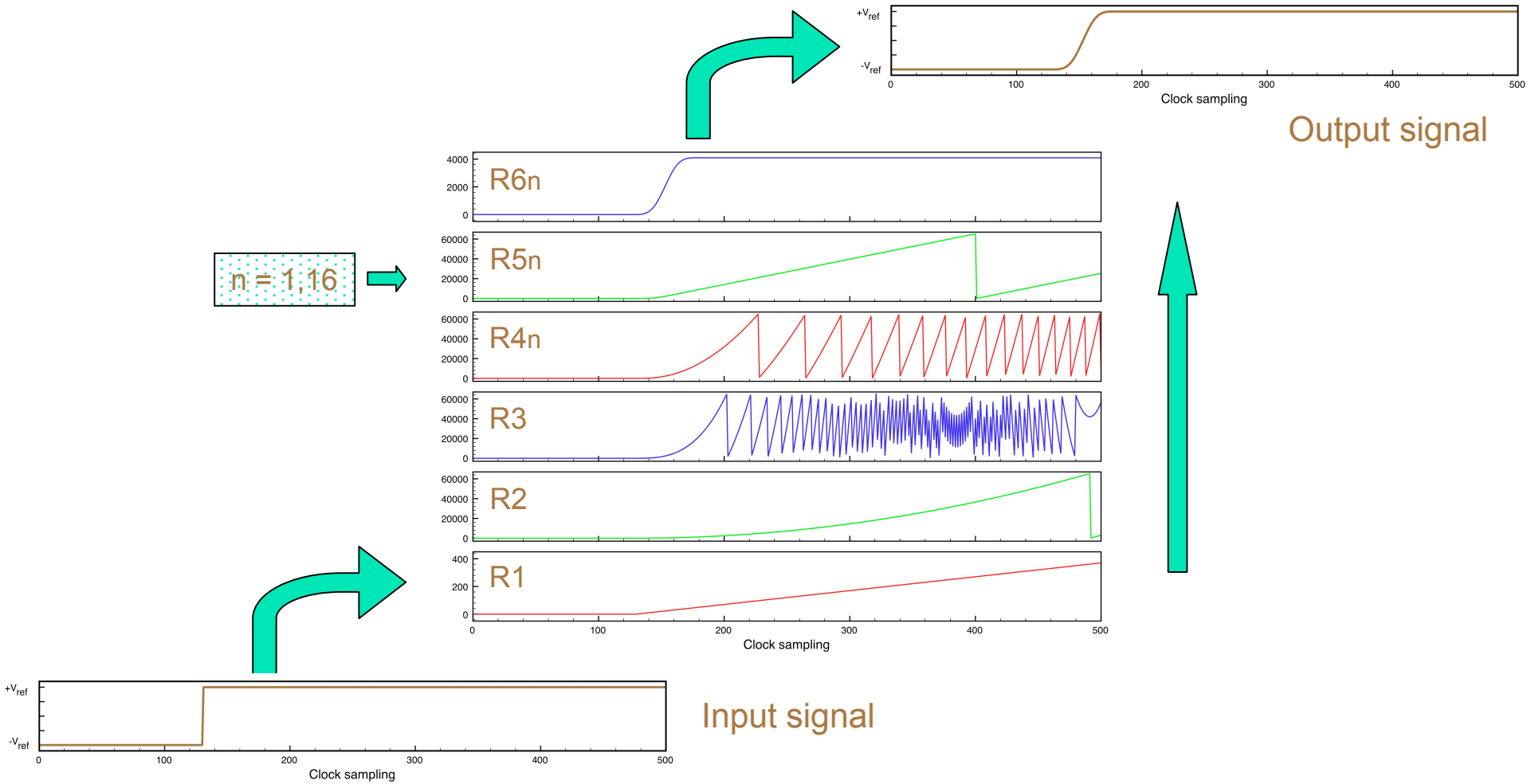
An interesting feature of this filter
is the possibility to reconstruct the data waveform
in an almost **continuous way**.
This feature could help in the data analysis,
where one could avoid fitting the data with
empirical analytical functions to extract the
deposited charge but rather use the numerical
integrals of the data themselves.

It is sufficient to modify the differentiation stages
adding stages up to the OSR value.

Filter & decimator



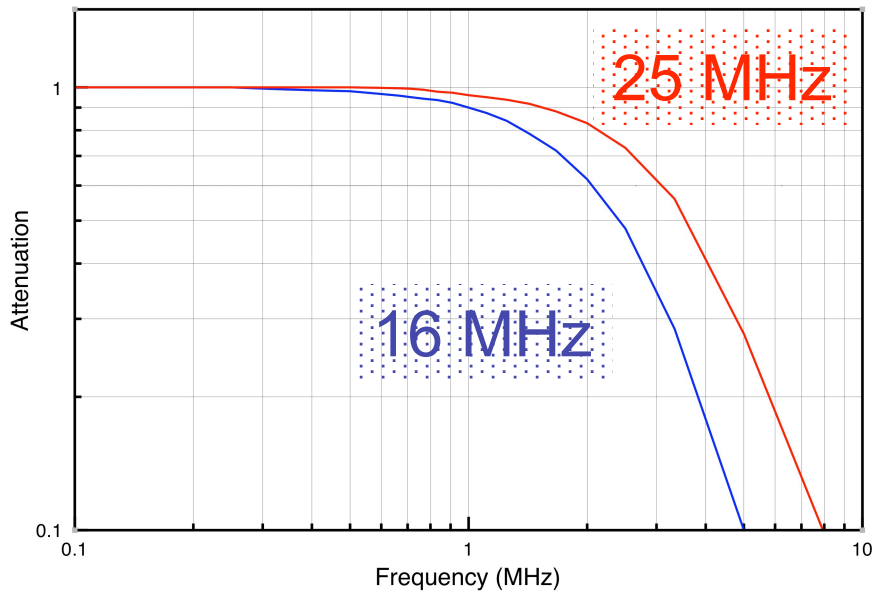
Continuous data reconstruction

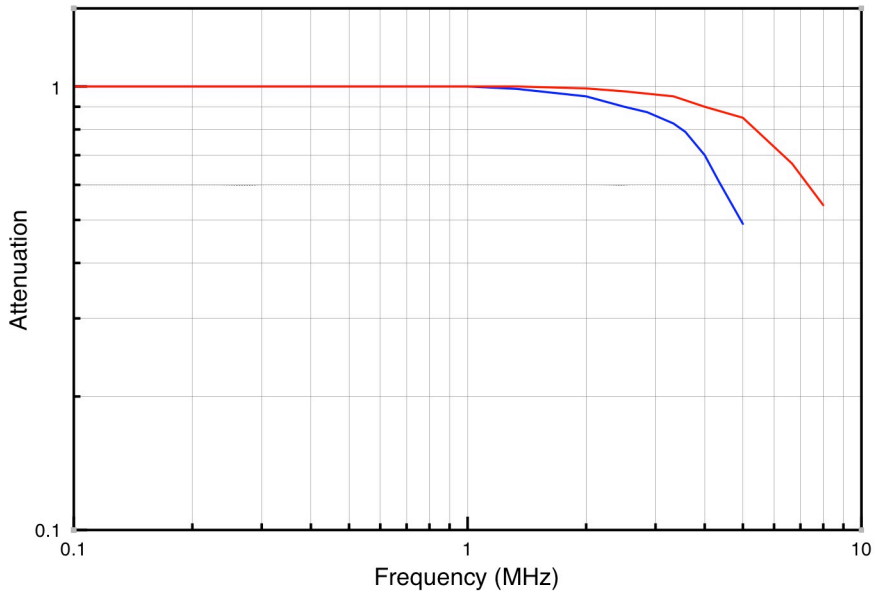


Filtered-ADC frequency response

16 sample FIR comb filter
equivalent to 10 bit resolution

8 sample FIR comb filter
equivalent to 8 bit resolution



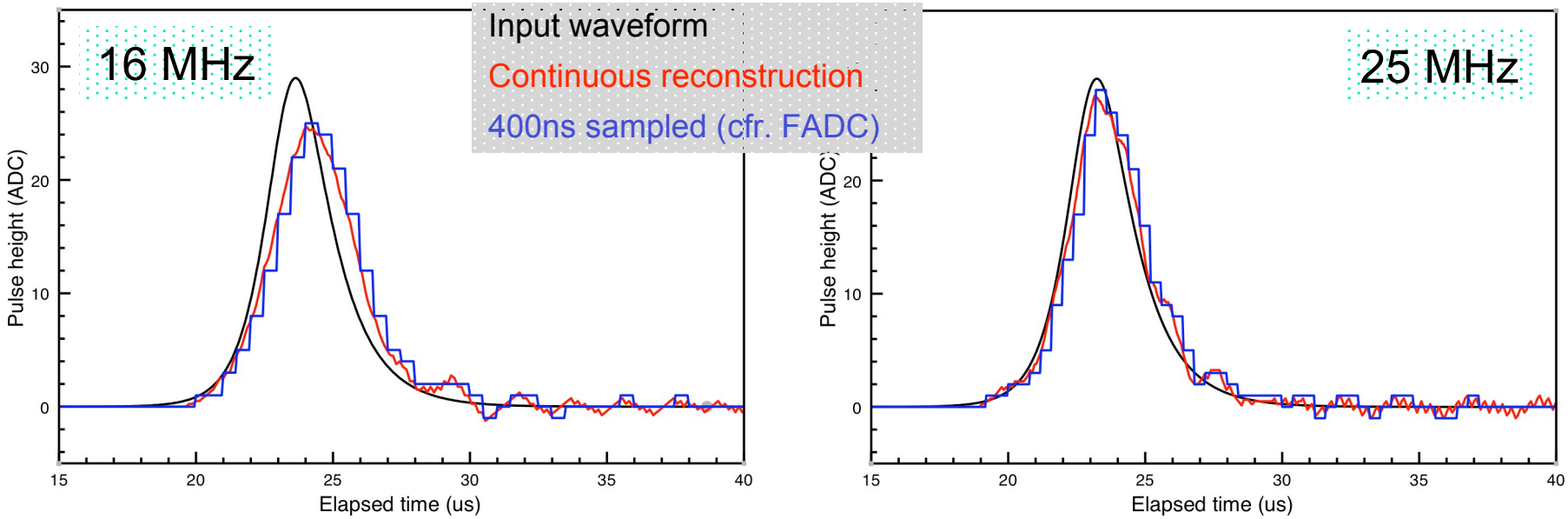


Compatible with typical ICARUS signal
bandwidth (< 1 MHz) also in 16 MHz case

max_f_in = 2 * samp_freq / fir_width
(Nyquist theorem)

Simulations

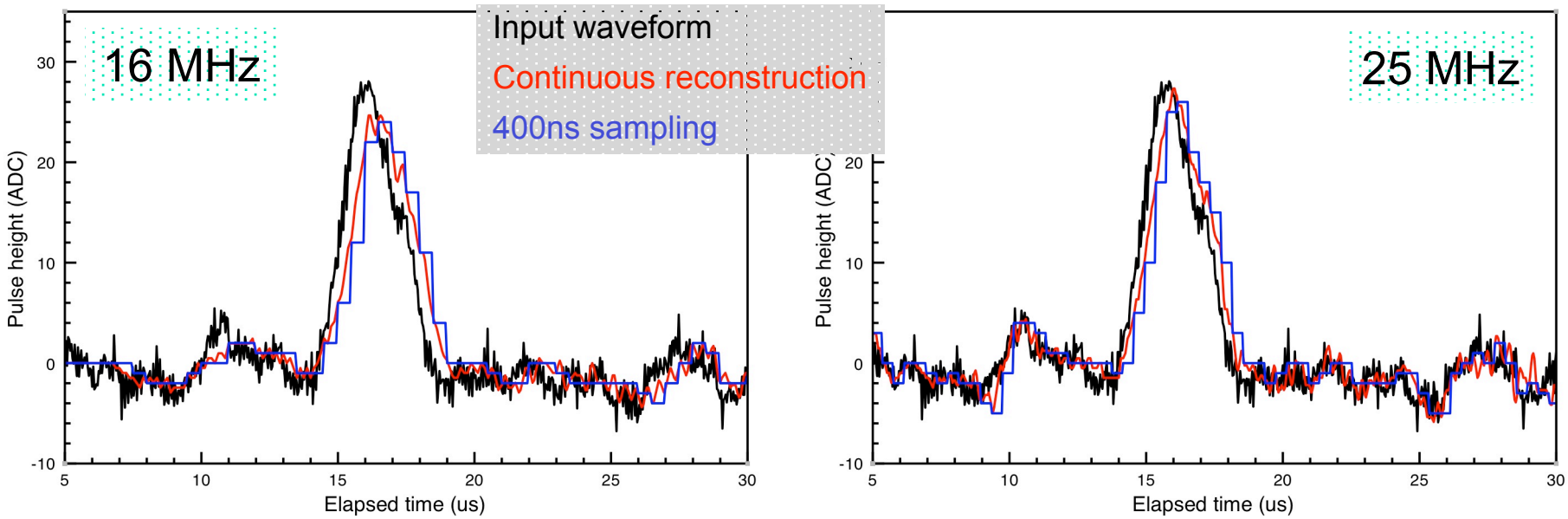
- Typical ICARUS signal waveform (~3 μs width) digitized with delta-sigma mod.
- FIR comb filter applied to recover signal shape (16 sample width)
  - 10 bit equivalent resolution
  - 1 bit quantization noise
  - Continuous reconstruction (useful feature for signal analysis)



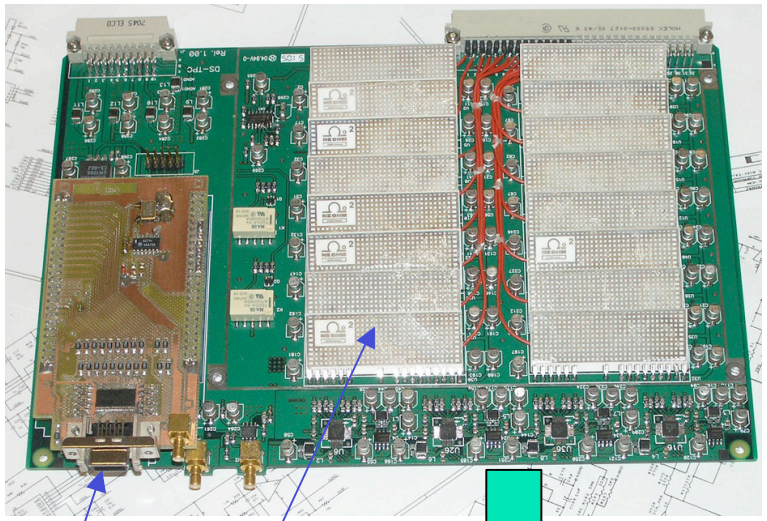
Slight pulse height reduction but area (= charge) unchanged

Signals from LAr

- LAr signal waveforms (from oscilloscope) digitized with sigma-delta AD converter simulator
- FIR comb filter applied to recover signal shape (16 sample width)
- Quantization noise well within analogue noise level

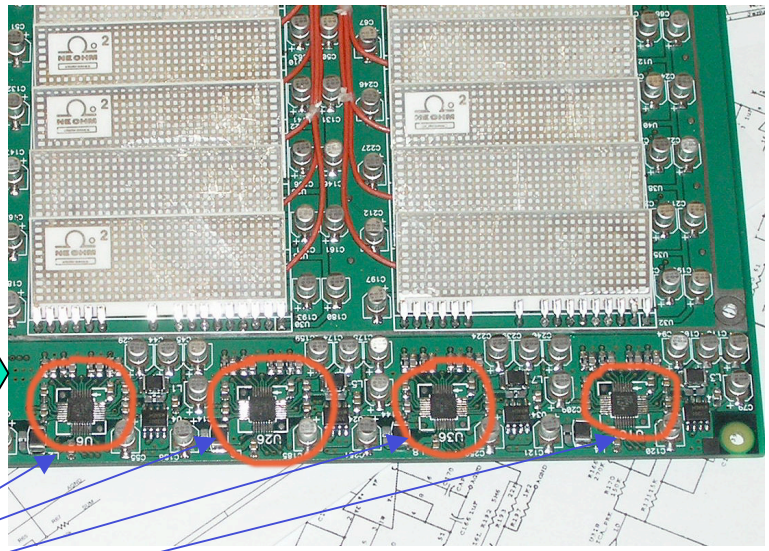


Prototype board



- 16 channels
- 16 MHz sampling rate
- Data link compatible with ICARUS DAQ
- Effective throughput 256 Mbit/s

Charge sensitive preamplifiers

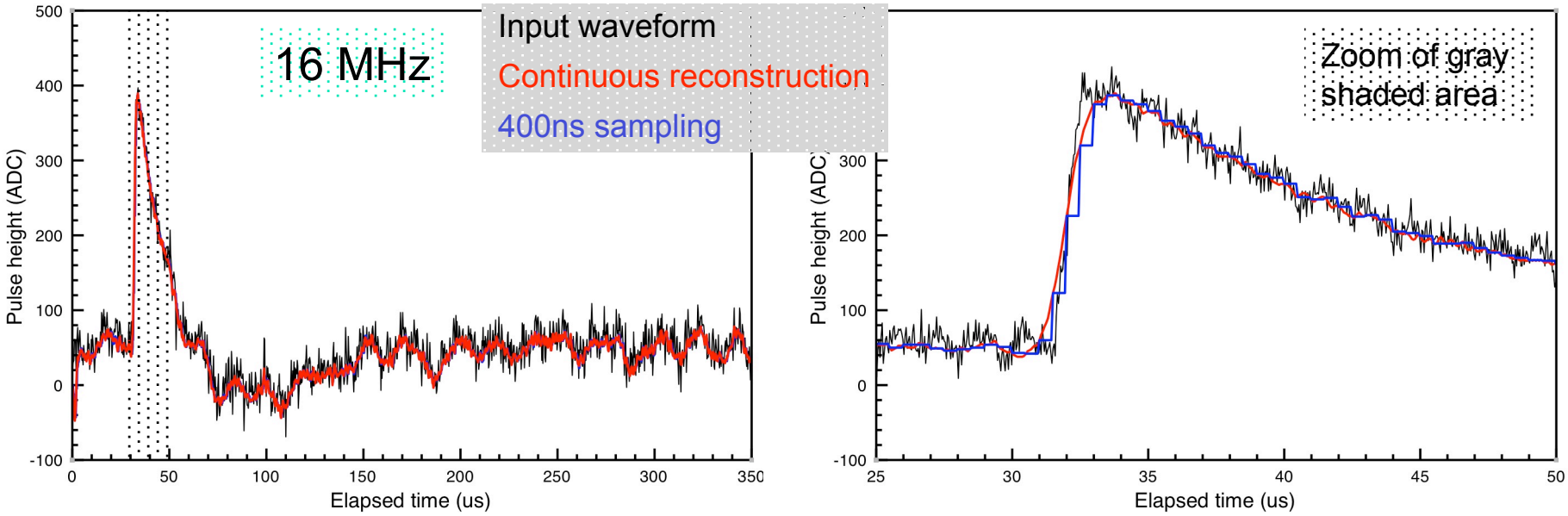


Digital link

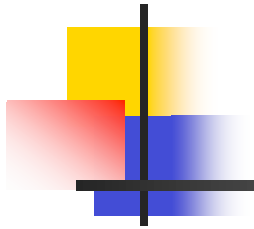
4 x 4 channel serial AD converters

First signals from **prototype**

- Test pulse injected on on-board preamplifiers
- Digitized signal recorded with ICARUS DAQ
- Off-line signal reconstruction with FIR comb filter (16 sample width)



High preamp. noise due to present board layout (analogue/digital interference)



New test system

New system modulo 64-chs, using PCI Express link at 2.5Gb/s on simple copper dual line.

“The new PCI Express Architecture comprehends a variety of form factors to support smooth integration with PCI and to enable new system form factors.”

“PCI Express Architecture will provide leading performance and price/performance.”

2.5Gb/s matches 64-chs @ 16MHz >> 1024Mb/s

Summary

- The ICARUS R&D on digital electronics for large LAr-TPC's:
  - Upgrade of Analogue-to-digital conversion
    - Sigma-delta: promising alternative to Multiplexer + Flash ACD
    - Intrinsically simpler,more compact, cheaper
    - Comparable bandwidth and signal resolution
  - Data link with digital buffers
    - PCI EXPRESS will be adopted
    - A system with ~500 channels soon available